US009306389B2

(12) **United States Patent**
Chuang

(10) **Patent No.: US 9,306,389 B2**
(45) **Date of Patent: Apr. 5, 2016**

(54) **ESD PROTECTION CIRCUIT**

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(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

(21) Appl. No.: **14/677,508**

(22) Filed: **Apr. 2, 2015**

(65) **Prior Publication Data**

US 2015/0214730 A1 Jul. 30, 2015

Related U.S. Application Data

(63) Continuation-in-part of application No. 13/742,854, filed on Jan. 16, 2013, now Pat. No. 9,001,479.

(60) Provisional application No. 61/595,933, filed on Feb. 7, 2012.

(51) **Int. Cl.**

H02H 9/00	(2006.01)
H02H 9/04	(2006.01)
H01L 27/02	(2006.01)
H03K 19/003	(2006.01)

(52) **U.S. Cl.**

CPC ***H02H 9/04*** (2013.01); ***H01L 27/0266*** (2013.01); ***H01L 27/0277*** (2013.01); ***H03K 19/00315*** (2013.01)

(58) **Field of Classification Search**

CPC H01L 27/0266
USPC 361/56
See application file for complete search history.

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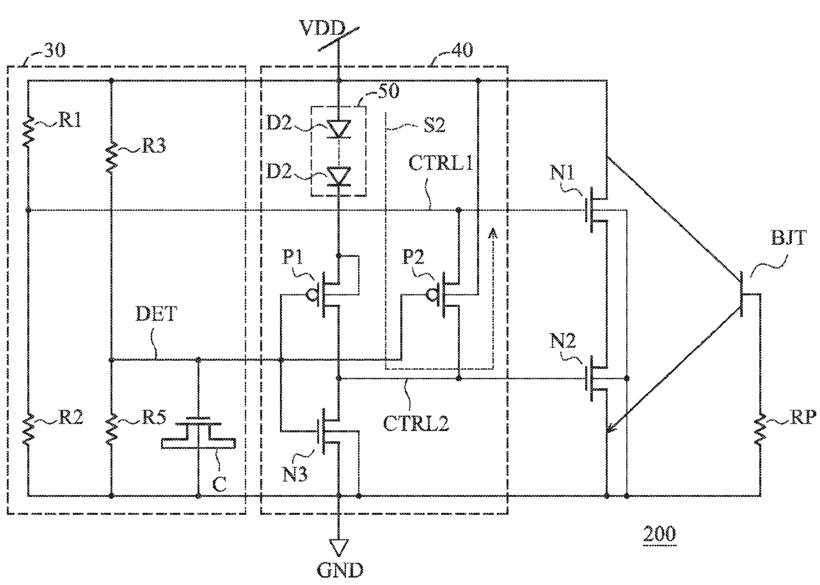
(57) **ABSTRACT**

An electrostatic discharge protection circuit is provided. First NMOS transistor is coupled to a power line. Second NMOS transistor is coupled between the first NMOS transistor and a ground. Detection unit provides a detection signal when an ESD event occurs at the power line. Trigger unit turns on the second NMOS transistor and the first NMOS transistor in sequence in response to the detection signal. Discharge path is formed from the power line to the ground via the first and second NMOS transistors. First PMOS transistor is coupled between the power line and a gate of the second NMOS transistor. Third NMOS transistor is coupled between the ground and the gate of the second NMOS transistor. Second PMOS transistor is coupled between the gates of the first and second NMOS transistors. Third PMOS transistor is coupled between the power line and the first PMOS transistor.

20 Claims, 9 Drawing Sheets



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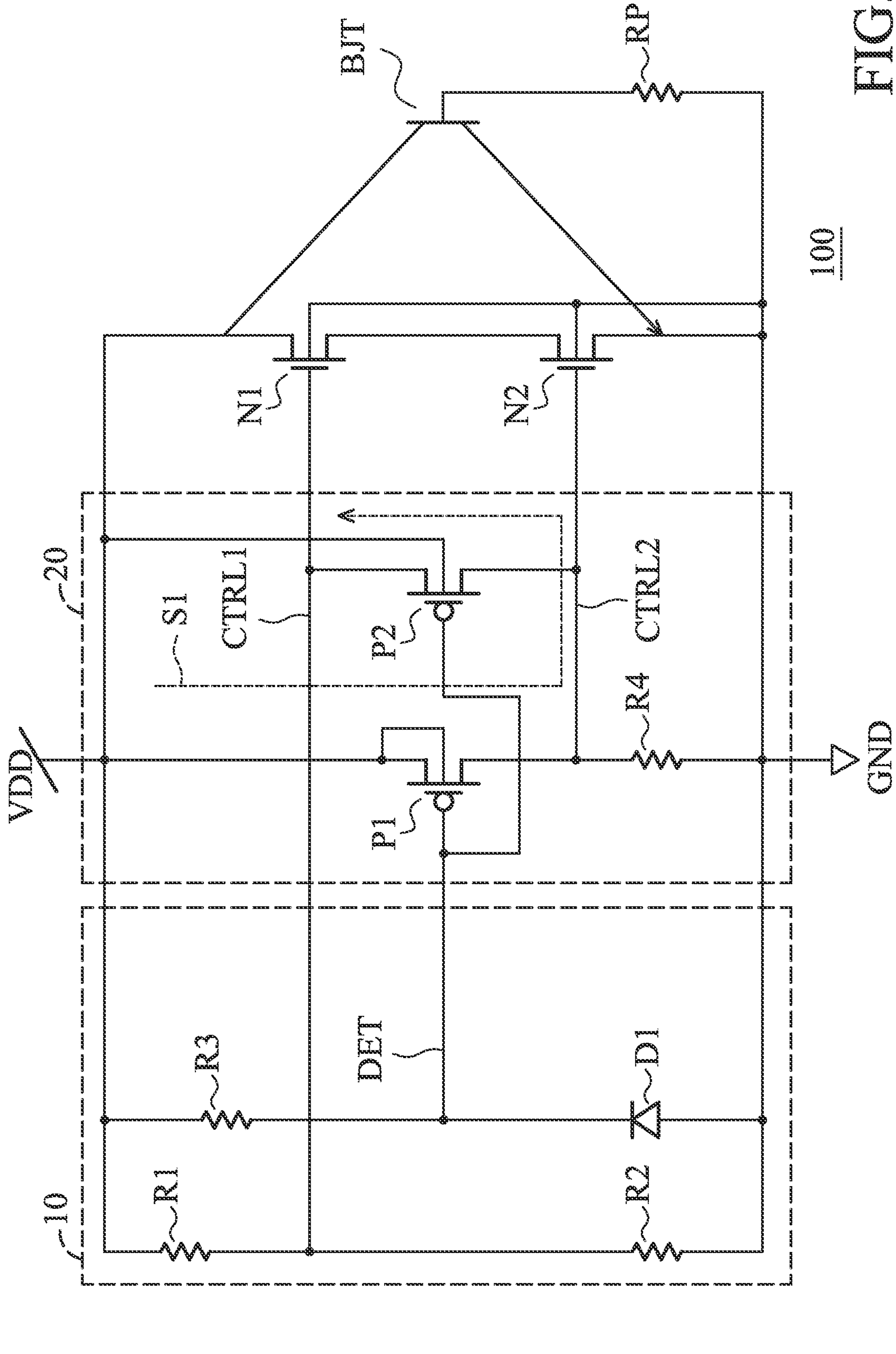


10
R1
R3
DET
D1
R2
20
S1
CTRL1
P2
P1
VDD
R4
GND
CTRL2
N1
N2
BJT
RP
100

FIG. 1

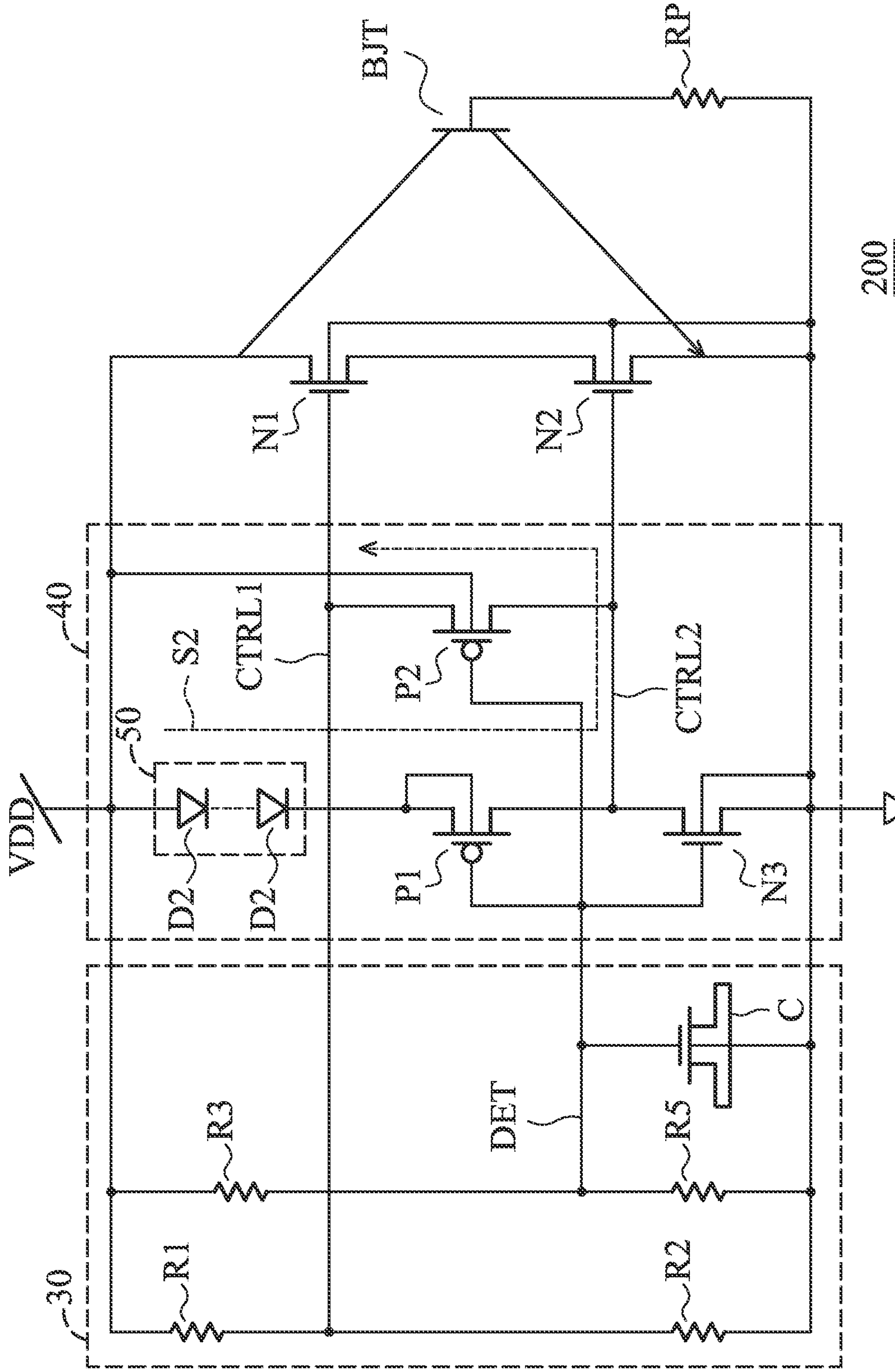
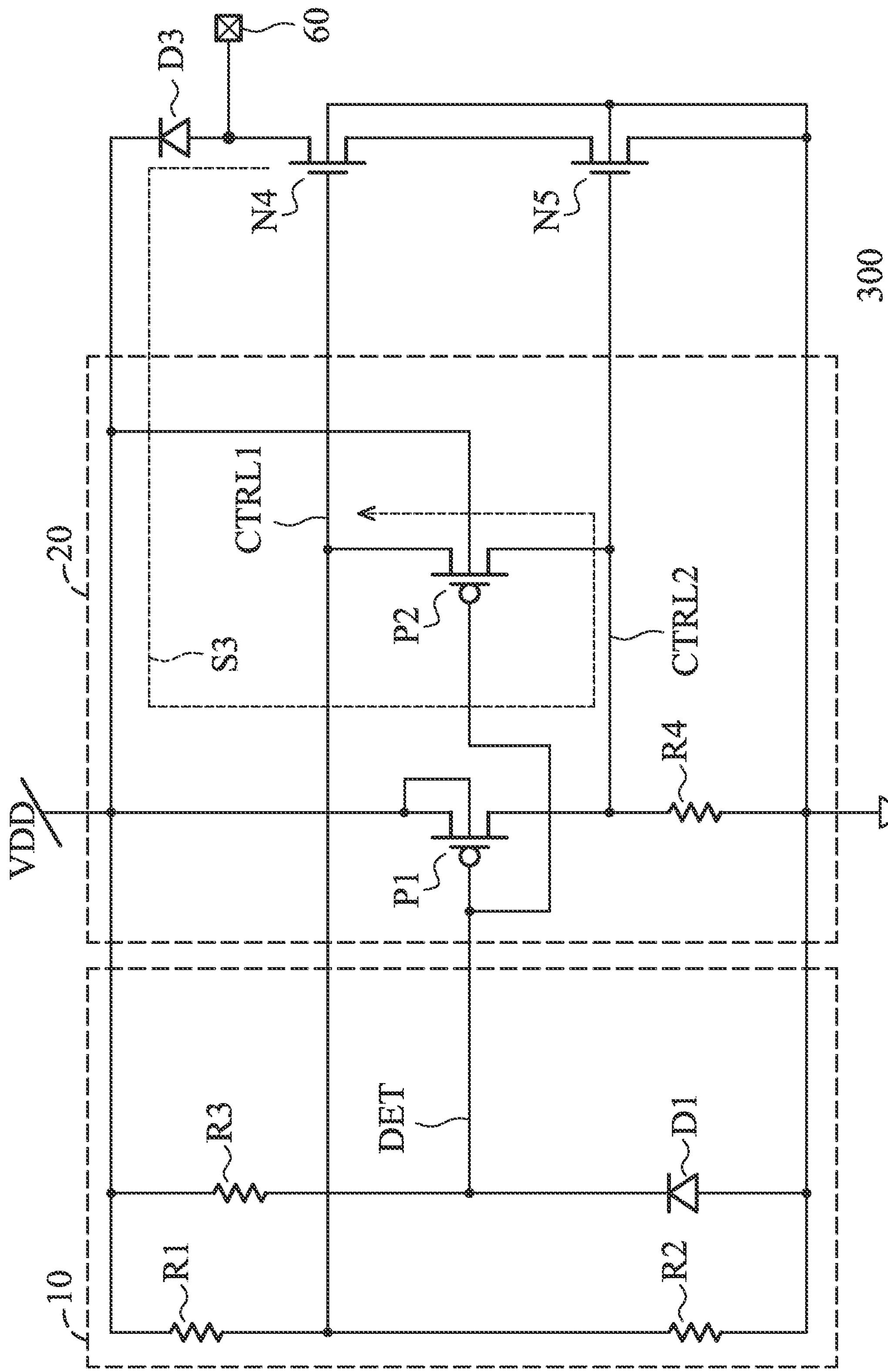
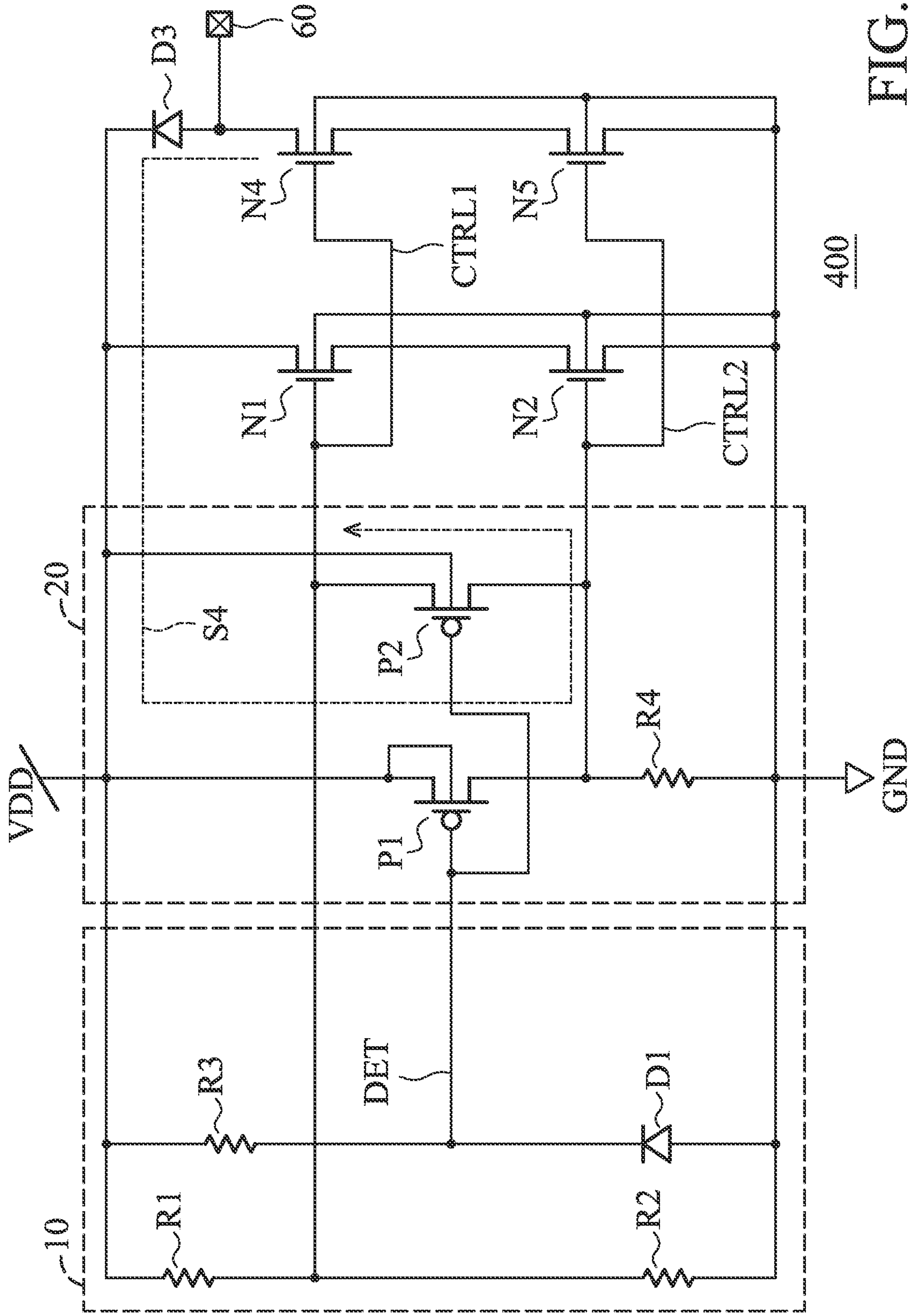

BJT
RP
200
N1
N2
40
S2
CTRL1
P2
CTRL2
50
VDD
D2
D2
P1
N3
GND
C
R3
DET
R5
R1
R2
30

FIG. 2



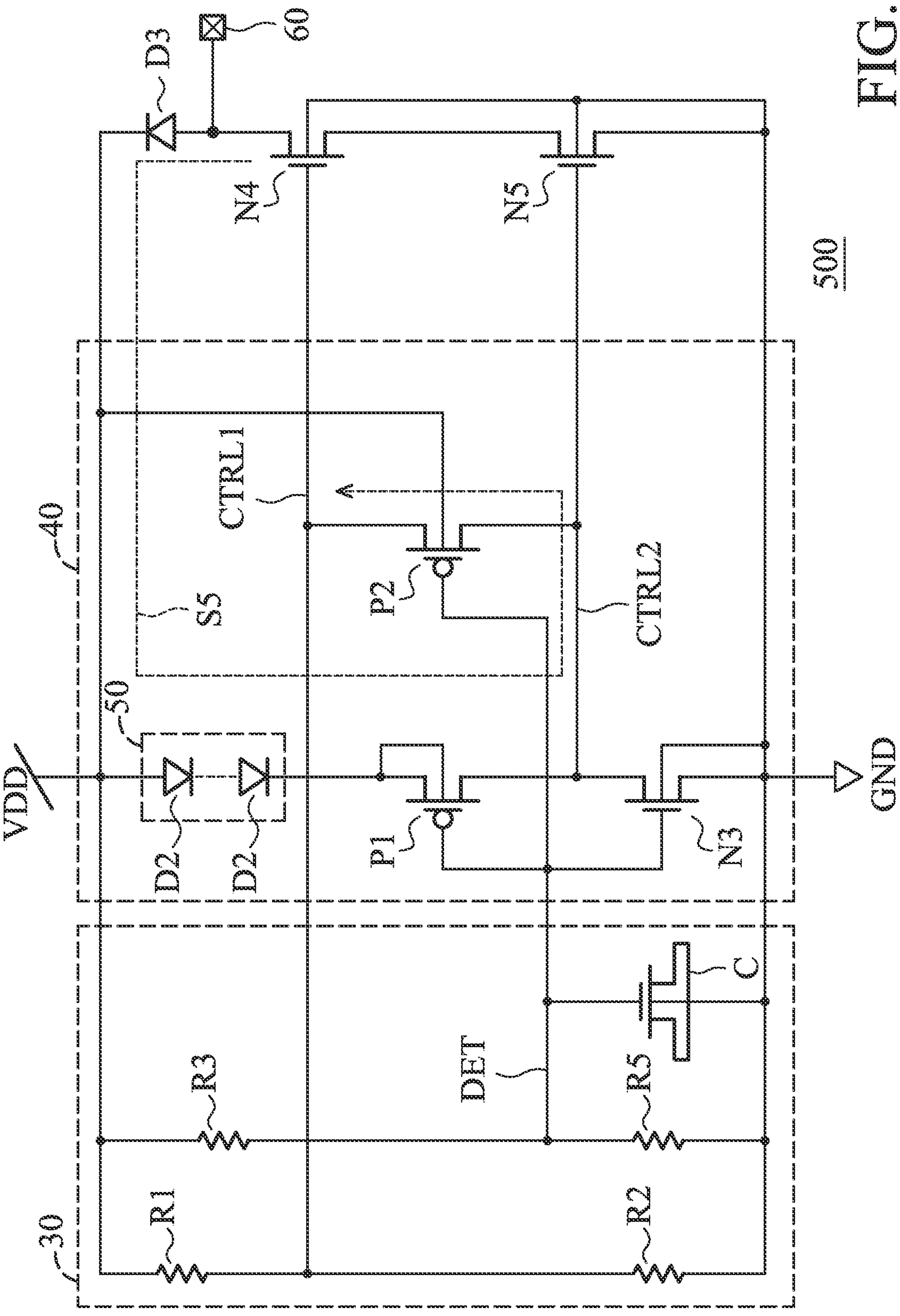
60
D3
N4
N5
300
20
CTRL1
CTRL2
S3
P2
P1
VDD
R4
GND
10
R1
R3
DET
D1
R2

FIG. 3



D3
60
N4
N5
CTRL1
400
N1
N2
CTRL2
20
S4
P2
VDD
P1
R4
GND
10
R3
DET
D1
R1
R2

FIG. 4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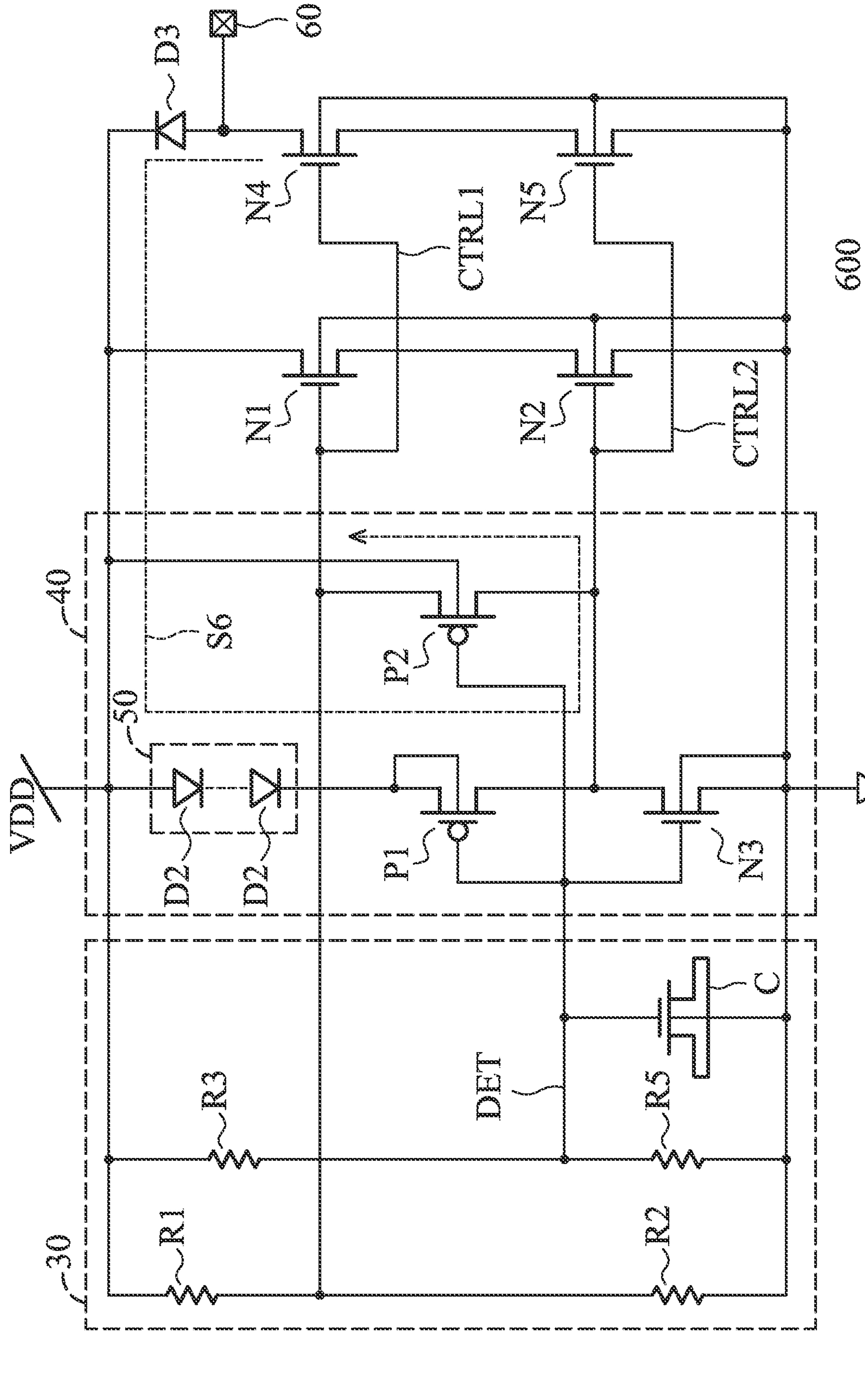
60
N4
N5
500
40
CTRL1
S5
P2
CTRL2
50
VDD
D2
D2
P1
N3
GND
C
DET
R3
R5
30
R1
R2

FIG. 5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60
N4
N5
CTRL1
600
N1
N2
CTRL2
40
S6
P2
50
VDD
D2
D2
P1
N3
GND
C
DET
R3
R5
30
R1
R2

FIG. 6

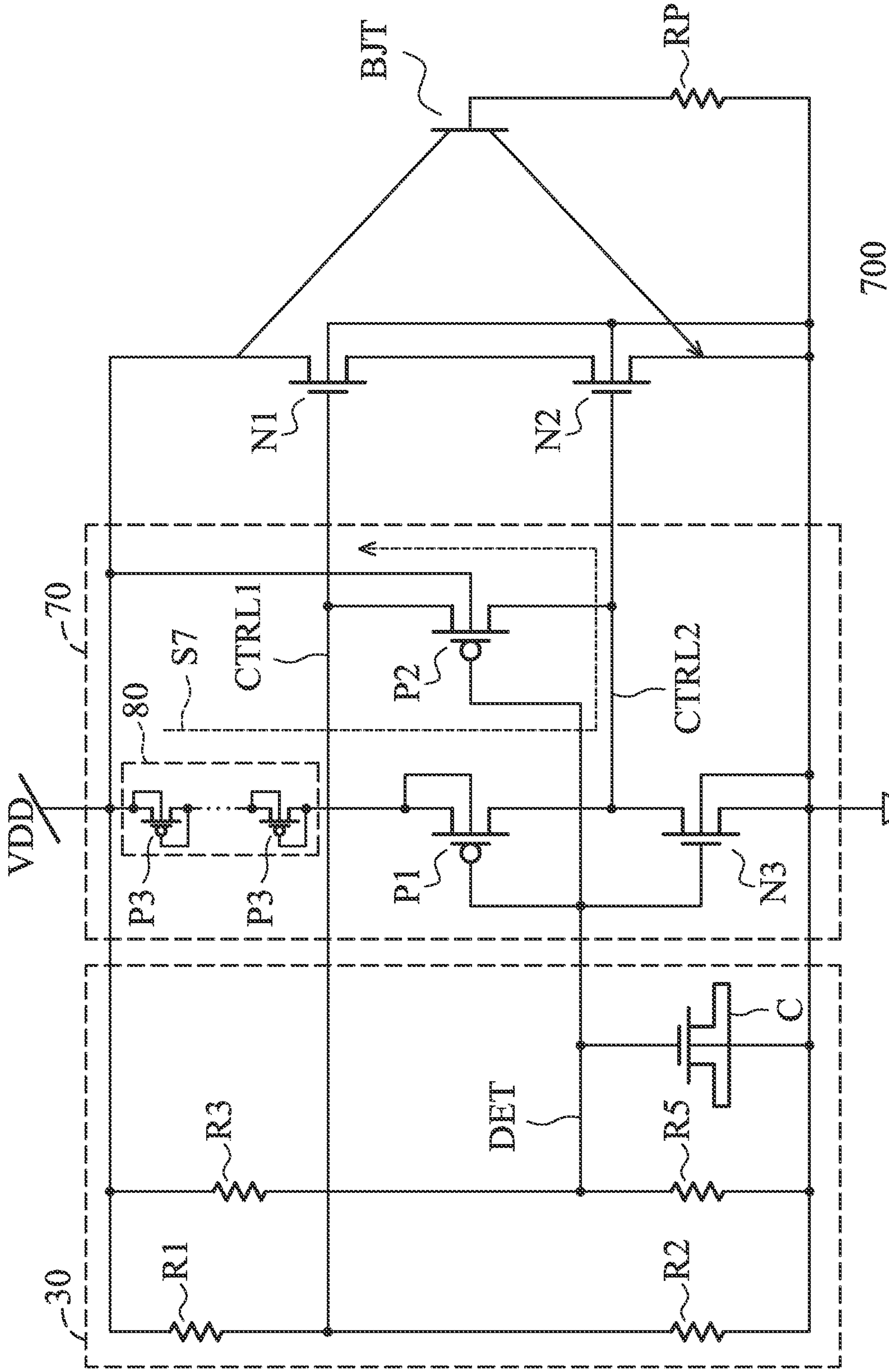
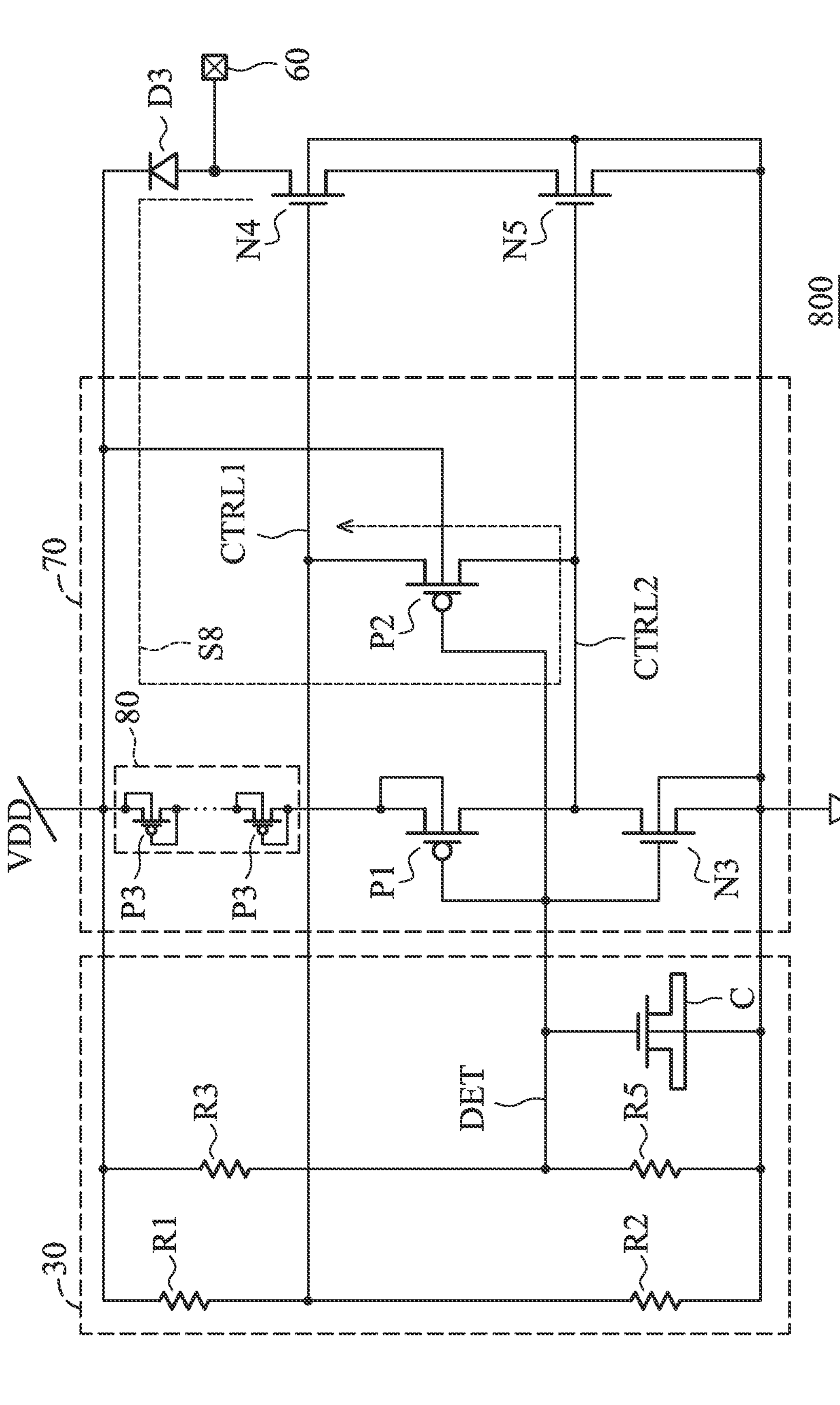

BJT
RP
700
N1
N2
70
S7
CTRL1
P2
CTRL2
80
VDD
P3
P3
P1
N3
GND
C
DET
R3
R5
R1
R2
30

FIG. 7



D3
60
N4
N5
800
70
CTRL1
CTRL2
P2
S8
80
VDD
P3
P3
P1
N3
GND
C
DET
R3
R5
R1
R2
30

FIG. 8

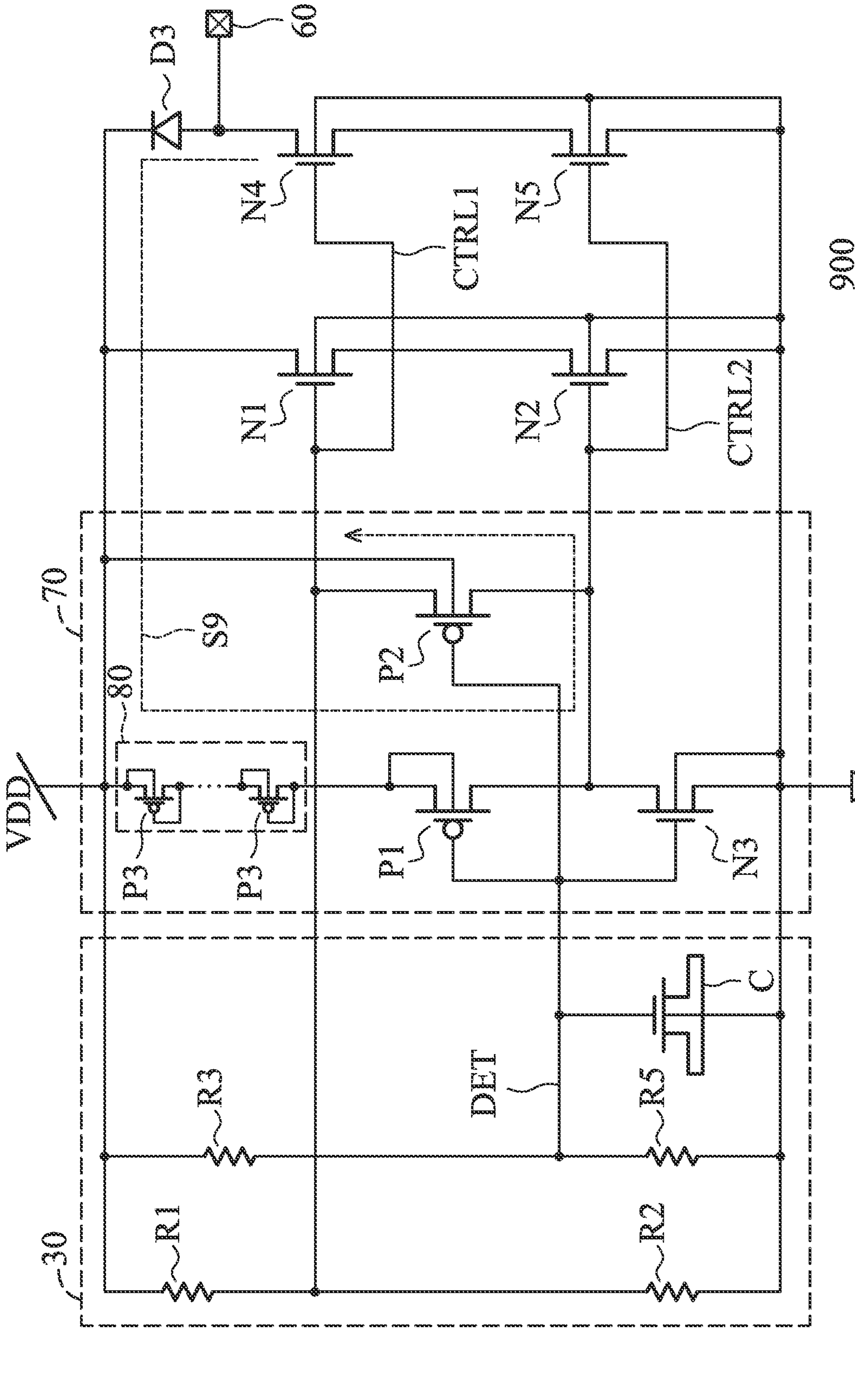

60
D3
N4
N5
CTRL1
900
N1
N2
CTRL2
70
S9
P2
80
VDD
P3
P3
P1
N3
GND
C
DET
R3
R5
R1
R2
30

FIG. 9

ESD PROTECTION CIRCUIT

CROSS REFERENCE TO RELATED APPLICATIONS

This application is a Continuation-In-Part of U.S. application Ser. No. 13/742,854, filed on Jan. 16, 2013, claims priority of U.S. Provisional Application No. 61/595,933, filed on Feb. 7, 2012, the entireties of which are incorporated by reference herein.

BACKGROUND OF THE INVENTION

1. Field of the Invention

The invention relates to an electrostatic discharge (ESD) protection circuit, and more particularly to an ESD protection circuit for a low-voltage process.

2. Description of the Related Art

Electrostatic discharge phenomena will cause damage to semiconductor devices and affect the normal functioning of integrated circuits (IC). Thus, it is a necessary goal for IC designers, during the design stage, to enhance ESD protection of an IC to increase ESD sensitivity.

Recently, more and more ICs can operate with lower operating voltages, such as operating voltages of typical logic circuits, i.e. 1.8V etc., due to the rapid advancement of low-voltage manufacturing technology. However, for certain products which have particular application requirements, certain pins for an IC require operating at higher voltages, i.e. 3V, 3.3V and so on.

For ICs, malfunctions will occur in low-voltage devices when a higher voltage is applied to the low-voltage devices. In this situation, the functions of the low-voltage device will be false since the low-voltage ESD protection circuit is unable to protect pins operating at higher voltages.

BRIEF SUMMARY OF THE INVENTION

Electrostatic discharge (ESD) protection circuits are provided. An embodiment of an ESD protection circuit is provided. The ESD protection circuit comprises: a first NMOS transistor coupled to a power line; a second NMOS transistor coupled between the first NMOS transistor and a ground; a detection unit, providing a detection signal when an ESD event occurs at the power line; and a trigger unit, turning on the second NMOS transistor and the first NMOS transistor in sequence in response to the detection signal, such that a discharge path is formed from the power line to the ground via the first and second NMOS transistors. The trigger unit comprises: a first PMOS transistor coupled between the power line and a gate of the second NMOS transistor, having a gate coupled to the detection unit for receiving the detection signal; a third NMOS transistor coupled between the ground and the gate of the second NMOS transistor, having a gate coupled to the gate of the first PMOS transistor; a second PMOS transistor coupled between a gate of the first NMOS transistor and the gate of the second NMOS transistor, having a gate coupled to the gate of the first PMOS transistor; and a third PMOS transistor coupled between the power line and the first PMOS transistor, having a drain, a gate, and a source, wherein the drain is coupled to the gate and the first PMOS transistor, and the source is coupled to the power line.

Furthermore, another embodiment of an ESD protection circuit is provided. The ESD protection circuit comprises: a diode, having an anode coupled to a pad and a cathode coupled to a power line; a first NMOS transistor coupled to the pad; a second NMOS transistor coupled between the first NMOS transistor and a ground; a detection unit coupled between the power line and the ground, providing a detection signal when an ESD event occurs at the pad; and a trigger unit coupled between the power line and the ground, turning on the second NMOS transistor and the first NMOS transistor in sequence in response to the detection signal, such that a first discharge path is formed from the pad to the ground through the first and second NMOS transistors. The trigger unit comprises: a first PMOS transistor coupled between the power line and a gate of the second NMOS transistor, having a gate coupled to the detection unit for receiving the detection signal; a third NMOS transistor coupled between the ground and the gate of the second NMOS transistor, having a gate coupled to the gate of the first PMOS transistor; a second PMOS transistor coupled between a gate of the first NMOS transistor and the gate of the second NMOS transistor, having a gate coupled to the gate of the first PMOS transistor; and a third PMOS transistor coupled between the power line and the first PMOS transistor, having a drain, a gate, and a source, wherein the drain is coupled to the gate and the first PMOS transistor, and the source is coupled to the power line.

Moreover, another embodiment of an ESD protection circuit is provided. The ESD protection circuit comprises: a first NMOS transistor coupled to a power line; a second NMOS transistor coupled between the first NMOS transistor and a ground; a detection unit, providing a detection signal when an ESD event occurs at the power line; and a trigger unit, turning on the second NMOS transistor and the first NMOS transistor in sequence in response to the detection signal, such that a discharge path is formed from the power line to the ground via the first and second NMOS transistors. The trigger unit comprises: a first PMOS transistor coupled between the power line and a gate of the second NMOS transistor, having a gate coupled to the detection unit for receiving the detection signal; a third NMOS transistor coupled between the ground and the gate of the second NMOS transistor, having a gate coupled to the gate of the first PMOS transistor; a second PMOS transistor coupled between a gate of the first NMOS transistor and the gate of the second NMOS transistor, having a gate coupled to the gate of the first PMOS transistor; and a plurality of third PMOS transistors coupled between the power line and the first PMOS transistor in serial, each having a drain, a gate, a source and a bulk, wherein the drain of the third PMOS transistor is coupled to the gate thereof, and the source of the third PMOS transistor is coupled to the bulk thereof.

Furthermore, another embodiment of an ESD protection circuit is provided. The ESD protection circuit comprises: a diode, having an anode coupled to a pad and a cathode coupled to a power line; a first NMOS transistor coupled to the pad; a second NMOS transistor coupled between the first NMOS transistor and a ground; a detection unit coupled between the power line and the ground, providing a detection signal when an ESD event occurs at the pad; and a trigger unit coupled between the power line and the ground, turning on the second NMOS transistor and the first NMOS transistor in sequence in response to the detection signal, such that a first discharge path is formed from the pad to the ground through the first and second NMOS transistors. The trigger unit comprises: a first PMOS transistor coupled between the power line and a gate of the second NMOS transistor, having a gate coupled to the detection unit for receiving the detection signal; a third NMOS transistor coupled between the ground and the gate of the second NMOS transistor, having a gate coupled to the gate of the first PMOS transistor; a second PMOS transistor coupled between a gate of the first NMOS transistor and the gate of the second NMOS transistor, having a gate coupled to the gate of the first PMOS transistor; and a plurality of third PMOS transistors coupled between the power line and the first PMOS transistor, each having a drain, a gate, a source and a bulk, wherein the drain of the third PMOS transistor is coupled to the gate thereof, and the source of the third PMOS transistor is coupled to the bulk thereof.

A detailed description is given in the following embodiments with reference to the accompanying drawings.

BRIEF DESCRIPTION OF DRAWINGS

The invention can be more fully understood by reading the subsequent detailed description and examples with references made to the accompanying drawings, wherein:

FIG. **1** shows an electrostatic discharge (ESD) protection circuit according to an embodiment of the invention;

FIG. **2** shows an ESD protection circuit according to another embodiment of the invention;

FIG. **3** shows an ESD protection circuit according to another embodiment of the invention;

FIG. **4** shows an ESD protection circuit according to another embodiment of the invention;

FIG. **5** shows an ESD protection circuit according to another embodiment of the invention;

FIG. **6** shows an ESD protection circuit according to another embodiment of the invention;

FIG. **7** shows an ESD protection circuit according to another embodiment of the invention;

FIG. **8** shows an ESD protection circuit according to another embodiment of the invention; and

FIG. **9** shows an ESD protection circuit according to another embodiment of the invention.

DETAILED DESCRIPTION OF THE INVENTION

The following description is of the best-contemplated mode of carrying out the invention. This description is made for the purpose of illustrating the general principles of the invention and should not be taken in a limiting sense. The scope of the invention is best determined by reference to the appended claims.

FIG. **1** shows an electrostatic discharge (ESD) protection circuit **100** according to an embodiment of the invention, wherein the ESD protection circuit **100** is implemented in an integrated circuit (IC). The ESD protection circuit **100** comprises the NMOS transistors N**1** and N**2**, a detection unit **10** and a trigger unit **20**. The detection unit **10** comprises the resistors R**1**, R**2** and R**3** and a diode D**1**. The resistor R**1** is coupled between a power line VDD and a gate of the NMOS transistor N**1**. The resistor R**2** is coupled between a ground GND and the gate of the NMOS transistor N**1**. The resistor R**3** is coupled between the power line VDD and the diode D**1**, wherein an anode of the diode D**1** is coupled to the resistor R**3** and a cathode of the diode D**1** is coupled to the ground GND. Furthermore, the diode D**1** can be any device type (p-n diode, MOS-connected diode and so on). The trigger unit **20** comprises the PMOS transistors P**1** and P**2** and a resistor R**4**. The PMOS transistor P**1** is coupled between the power line VDD and a gate of the NMOS transistor N**2**. The PMOS transistor P**2** is coupled between the gates of the NMOS transistors N**1** and N**2**. The gates of the PMOS transistor P**1** and P**2** are coupled to the cathode of the diode D**1** for receiving a detection signal DET, and the bulks of the PMOS transistors P**1** and P**2** are coupled to the power line VDD. In the embodiment, the NMOS transistors N**1** and N**2** are stacked NMOS transistors for reliability, wherein the NMOS transistor N**1** is coupled between the power line VDD and the NMOS transistor N**2** and the NMOS transistor N**2** is coupled between the NMOS transistor N**1** and the ground GND. The gate of the NMOS transistor N**1** is controlled by a control signal CTRL**1**, and the gate of the NMOS transistor N**2** is controlled by a control signal CTRL**2**, wherein the bulks of the NMOS transistors N**1** and N**2** are coupled to the ground GND.

In FIG. **1**, the NMOS transistor N**1** and N**2** and the PMOS transistors P**1** and P**2** are low-voltage devices (e.g. 1.8V), and a higher fixed voltage (e.g. 3.3V) is applied to the power line VDD via a power pad of the IC. In normal mode, the control signal CTRL**1** is determined according to a voltage division between the resistors R**1** and R**2**, e.g. if R**1**=R**2**, CTRL**1**=VDD/2. Thus, the NMOS transistor N**1** is turned on. Furthermore, the detection signal DET is determined according to a voltage of the power line VDD due to the diode D**1** being off. Therefore, the PMOS transistors P**1** and P**2** are turned off, and then the control signal CTRL**2** is pulled down to the ground GND via the resistor R**4**. Thus, the NMOS transistor N**2** is turned off. When an ESD event occurs at the power line VDD, the detection unit **10** provides the detection signal DET in response to the ESD event to turn on the PMOS transistors P**1** and P**2**. Next, a portion of ESD energy from the power line VDD passes through the PMOS transistor P**1** to turn on the NMOS transistor N**2**, and then passed through the PMOS transistor P**2** to turn on the NMOS transistor N**1**, as shown in label S**1**. Therefore, a discharge path is formed from the power line VDD to the ground GND via the NMOS transistors N**1** and N**2** in an ESD mode, such that the electrical devices of the IC coupled to the power line VDD will be prevented from ESD damage. Furthermore, a parasitic bipolar transistor BJT and a parasitic resistor RP may further provide an additional discharge path for the ESD protection circuit **100**.

FIG. **2** shows an ESD protection circuit **200** according to another embodiment of the invention, wherein the ESD protection circuit **200** is implemented in an IC. The ESD protection circuit **200** comprises the NMOS transistors N**1** and N**2**, a detection unit **30** and a trigger unit **40**. The detection unit **30** comprises the resistors R**1**, R**2**, R**3** and R**5** and a capacitor C, wherein the capacitor C is formed by an NMOS transistor. The resistor R**1** is coupled between the power line VDD and a gate of the NMOS transistor N**1**. The resistor R**2** is coupled between the ground GND and the gate of the NMOS transistor N**1**. The resistor R**3** is coupled between the power line VDD and the resistor R**5**. The resistor R**5** is coupled between the resistor R**3** and the ground GND. The capacitor C is coupled to the resistor R**5** in parallel. The trigger unit **40** comprises the PMOS transistors P**1** and P**2**, an NMOS transistor N**3** and a diode chain **50**. The diode chain **50** is coupled between the power line VDD and the PMOS transistor P**1**, which comprises a plurality of diodes D**2**. Each diode D**2** is coupled in a forward conduction direction from the power line VDD to the PMOS transistor P**1**. Furthermore, each diode D**2** can be any device type (p-n diode, MOS-connected diode and so on). The amount of the diodes D**2** is determined according to actual applications. For example, a forward bias voltage of the diode chain **50** plus a threshold voltage of the PMOS transistor P**1** equals a voltage of the detection signal DET. In one embodiment, the diode chain **50** may only comprise a single diode D**2**. The PMOS transistor P**1** is coupled between the diode chain **50** and a gate of the NMOS transistor N**2**. The PMOS transistor P**2** is coupled between the gates of the NMOS transistors N**1** and N**2**. The gates of the PMOS transistor P**1** and P**2** are coupled to the capacitor C for receiving a detection signal DET, and the bulks of the PMOS transistors P**1** and P**2** are coupled to the diode chain **50** and the power line VDD, respectively. The NMOS transistor N**3** is coupled between the PMOS transistor P1 and the ground GND, wherein a gate of the NMOS transistor N3 is coupled to the capacitor C for receiving the detection signal DET. Similarly, the NMOS transistors N1 and N2 are stacked NMOS transistors for reliability, wherein the NMOS transistor N1 is coupled between the power line VDD and the NMOS transistor N2 and the NMOS transistor N2 is coupled between the NMOS transistor N1 and the ground GND. The gate of the NMOS transistor N1 is controlled by a control signal CTRL1, and the gate of the NMOS transistor N2 is controlled by a control signal CTRL2, wherein the bulks of the NMOS transistors N1 and N2 are coupled to the ground GND.

In FIG. 2, the NMOS transistor N1, N2 and N3 and the PMOS transistors P1 and P2 are low-voltage devices (e.g. 1.8V), and a higher fixed voltage (e.g. 3.3V) is applied to the power line VDD via a power pad of the IC. In normal mode, the control signal CTRL1 is determined according to a voltage division between the resistors R1 and R2, e.g. if R1=R2, CTRL1=VDD/2. Thus, the NMOS transistor N1 is turned on. Furthermore, the detection signal DET is determined according to a voltage division between the resistors R3 and R5, e.g. if R3=R5, DET=VDD/2. Therefore, the PMOS transistors P1 and P2 are turned off and the NMOS transistor N3 is turned on, and then the control signal CTRL2 is pulled down to the ground GND via the NMOS transistor N3. Thus, the NMOS transistor N2 is turned off. When an ESD event occurs at the power line VDD, the detection unit 30 provides the detection signal DET in response to the ESD event, to turn on the PMOS transistors P1 and P2 and to turn off the NMOS transistor N3. Next, a portion of ESD energy from the power line VDD passes through the diode chain 50 and the PMOS transistor P1, to turn on the NMOS transistor N2, and then passes through the PMOS transistor P2 to turn on the NMOS transistor N1, as shown in label S2. Therefore, a discharge path is formed from the power line VDD to the ground GND via the NMOS transistors N1 and N2 in ESD mode, such that the electrical devices of the IC coupled to the power line VDD will be prevented from ESD damage. Furthermore, a parasitic bipolar transistor BJT and a parasitic resistor RP may provide an additional discharge path for the ESD protection circuit 200.

FIG. 3 shows an ESD protection circuit 300 according to another embodiment of the invention, wherein the ESD protection circuit 300 is implemented in an IC. Compared to the ESD protection circuit 100 of FIG. 1, the ESD protection circuit 300 is used to provide ESD protection for an input/output (I/O) pad 60 of the IC. The ESD protection circuit 300 comprises a diode D3, the NMOS transistors N4 and N5, a detection unit 10 and a trigger unit 20, wherein details of the detection unit 10 and the trigger unit 20 are described above. An anode of the diode D3 is coupled to the I/O pad 60 and a cathode of the diode D3 is coupled to the power line VDD. Furthermore, the diode D3 can be any device type (p-n diode, MOS-connected diode and so on). The NMOS transistor N4 is coupled between the anode of the diode D3 and the NMOS transistor N5, which has a gate coupled to the resistors R1 and R2 and the PMOS transistor P2 for receiving the control signal CTRL1. The NMOS transistor N5 is coupled between the NMOS transistor N4 and the ground GND, which has a gate coupled to the resistor R4 and the PMOS transistors P1 and P2 for receiving the control signal CTRL2. The bulks of the NMOS transistors N4 and N5 are coupled to the ground GND.

In FIG. 3, the NMOS transistor N4 and N5 and the PMOS transistors P1 and P2 are low-voltage devices (e.g. 1.8V), and a higher fixed voltage (e.g. 3.3V) is applied to the power line VDD via a power pad of the IC. In normal mode, the control signal CTRL1 is determined according to a voltage division between the resistors R1 and R2, e.g. if R1=R2, CTRL1=VDD/2. Thus, the NMOS transistor N4 is turned on. Furthermore, the detection signal DET is determined according to the voltage of the power line VDD due to the diode D1 being off. Therefore, the PMOS transistors P1 and P2 are turned off, and then the control signal CTRL2 is pulled down to the ground GND via the resistor R4. Thus, the NMOS transistor N5 is turned off. When an ESD event occurs at the I/O pad 60, a portion of ESD energy from the I/O pad 60 passes through the diode D3 to the power line VDD. Therefore, the detection unit 10 provides the detection signal DET in response to the ESD event, to turn on the PMOS transistors P1 and P2. When the ESD event occurs at the I/O pad 60, a portion of ESD energy from the I/O pad 60 sequentially passes through the diode D3, the power line VDD and the PMOS transistor P1, to turn on the NMOS transistor N5, and then passes through the PMOS transistor P2 to turn on the NMOS transistor N4, as shown in label S3. Therefore, a discharge path is formed from the I/O pad 60 to the ground GND via the NMOS transistors N4 and N5 in an ESD mode, such that the electrical devices of the IC coupled to the power line VDD will be prevented from ESD damage. Similarly, a parasitic bipolar transistor and a parasitic resistor may further provide an additional discharge path for the ESD protection circuit 300.

FIG. 4 shows an ESD protection circuit 400 according to another embodiment of the invention, wherein the ESD protection circuit 400 is implemented in an IC. Compared to the ESD protection circuit 300 of FIG. 3, the ESD protection circuit 400 further comprises the NMOS transistors N1 and N2. The NMOS transistor N1 is coupled between the power line VDD and the NMOS transistor N2, which has a gate coupled to the gate of the NMOS transistor N4. The NMOS transistor N2 is coupled between the NMOS transistor N1 and the ground GND, which has a gate coupled to the gate of the NMOS transistor N5. In FIG. 4, the NMOS transistor N1, N2, N4 and N5 and the PMOS transistors P1 and P2 are low-voltage devices (e.g. 1.8V), and a higher fixed voltage (e.g. 3.3V) is applied to the power line VDD via a power pad of the IC. In normal mode, the control signal CTRL1 is determined according to a voltage division between the resistors R1 and R2, e.g. if R1=R2, CTRL1=VDD/2. Thus, the NMOS transistors N1 and N4 are turned on. Furthermore, the detection signal DET is determined according to the voltage of the power line VDD due to the diode D1 being off. Therefore, the PMOS transistors P1 and P2 are turned off, and then the control signal CTRL2 is pulled down to the ground GND via the resistor R4. Thus, the NMOS transistors N2 and N5 are turned off. When an ESD event occurs at the I/O pad 60, a portion of ESD energy from the I/O pad 60 passes through the diode D3 to the power line VDD. Therefore, the detection unit 10 provides the detection signal DET in response to the ESD event, to turn on the PMOS transistors P1 and P2. When the ESD event occurs at the I/O pad 60, a portion of ESD energy from the I/O pad 60 sequentially passes through the diode D3, the power line VDD and the PMOS transistor P1 to turn on the NMOS transistors N2 and N5, and then passes through the PMOS transistor P2 to turn on the NMOS transistors N1 and N4, as shown in label S4. In an ESD mode, a first discharge path is formed from the I/O pad 60 to the ground GND via the NMOS transistors N4 and N5, and a second discharge path is formed from the I/O pad 60 to the ground GND via the diode D3 and the NMOS transistors N4 and N5. Thus, the electrical devices of the IC coupled to the power line VDD will be prevented from ESD damage. Similarly, the parasitic bipolar transistors and the parasitic resistors may provide additional discharge paths for the ESD protection circuit **400**.

FIG. **5** shows an ESD protection circuit **500** according to another embodiment of the invention, wherein the ESD protection circuit **500** is implemented in an IC. Compared to the ESD protection circuit **200** of FIG. **2**, the ESD protection circuit **500** is used to provide ESD protection for an I/O pad **60** of the IC. The ESD protection circuit **500** comprises a diode D**3**, the NMOS transistors N**4** and N**5**, a detection unit **30** and a trigger unit **40**, wherein details of the detection unit **30** and the trigger unit **40** are described above. An anode of the diode D**3** is coupled to the I/O pad **60** and a cathode of the diode D**3** is coupled to the power line VDD. The NMOS transistor N**4** is coupled between the anode of the diode D**3** and the NMOS transistor N**5**, which has a gate coupled to the resistors R**1** and R**2** and the PMOS transistor P**2** for receiving the control signal CTRL**1**. The NMOS transistor N**5** is coupled between the NMOS transistor N**4** and the ground GND, which has a gate coupled to the NMOS transistor N**3** and the PMOS transistors P**1** and P**2** for receiving the control signal CTRL**2**.

In FIG. **5**, the NMOS transistors N**4** and N**5** and the PMOS transistors P**1** and P**2** are low-voltage devices (e.g. 1.8V), and a higher fixed voltage (e.g. 3.3V) is applied to the power line VDD via a power pad of the IC. In normal mode, the control signal CTRL**1** is determined according to a voltage division between the resistors R**1** and R**2**, e.g. if R**1**=R**2**, CTRL**1**=VDD/2. Thus, the NMOS transistor N**4** is turned on. Furthermore, the detection signal DET is determined according to a voltage division between the resistors R**3** and R**5**, e.g. if R**3**=R**5**, DET=VDD/2. Therefore, the PMOS transistors P**1** and P**2** are turned off and the NMOS transistor N**3** is turned on, and then the control signal CTRL**2** is pulled down to the ground GND via the NMOS transistor N**3**. Thus, the NMOS transistor N**5** is turned off. When an ESD event occurs at the I/O pad **60**, a portion of ESD energy from the I/O pad **60** passes through the diode D**3** to the power line VDD. Therefore, the detection unit **30** provides the detection signal DET in response to the ESD event, to turn on the PMOS transistors P**1** and P**2** and to turn off the NMOS transistor N**3**. When the ESD event occurs at the I/O pad **60**, a portion of ESD energy the I/O pad **60** sequentially passes through the diode D**3**, the power line VDD, the diode chain **50** and the PMOS transistor P**1**, to turn on the NMOS transistor N**5**, and then passes through the PMOS transistor P**2** to turn on the NMOS transistor N**4**, as shown in label S**5**. Therefore, a discharge path is formed from the I/O pad **60** to the ground GND via the NMOS transistors N**4** and N**5** in an ESD mode, such that the electrical devices of the IC coupled to the power line VDD will be prevented from ESD damage. Similarly, a parasitic bipolar transistor and a parasitic resistor may further provide an additional discharge path for the ESD protection circuit **500**.

FIG. **6** shows an ESD protection circuit **600** according to another embodiment of the invention, wherein the ESD protection circuit **600** is implemented in an IC. Compared to the ESD protection circuit **500** of FIG. **5**, the ESD protection circuit **600** further comprises the NMOS transistors N**1** and N**2**. The NMOS transistor N**1** is coupled between the power line VDD and the NMOS transistor N**2**, which has a gate coupled to the gate of the NMOS transistor N**4**. The NMOS transistor N**2** is coupled between the NMOS transistor N**1** and the ground GND, which has a gate coupled to the gate of the NMOS transistor N**5**. In FIG. **6**, the NMOS transistors N**1**, N**2**, N**4** and N**5** and the PMOS transistors P**1** and P**2** are low-voltage devices (e.g. 1.8V), and a higher fixed voltage (e.g. 3.3V) is applied to the power line VDD via a power pad of the IC. In normal mode, the control signal CTRL**1** is determined according to a voltage division between the resistors R**1** and R**2**, e.g. if R**1**=R**2**, CTRL**1**=VDD/2. Thus, the NMOS transistors N**1** and N**4** are turned on. Furthermore, the detection signal DET is determined according to a voltage division between the resistors R**3** and R**5**, e.g. if R**3**=R**5**, DET=VDD/2. Therefore, the PMOS transistors P**1** and P**2** are turned off and the NMOS transistor N**3** is turned on, and then the control signal CTRL**2** is pulled down to the ground GND via the NMOS transistor N**3**. Thus, the NMOS transistors N**2** and N**5** are turned off. When an ESD event occurs at the I/O pad **60**, a portion of ESD energy from the I/O pad **60** passes through the diode D**3** to the power line VDD. Therefore, the detection unit **30** provides the detection signal DET in response to the ESD event, to turn on the PMOS transistors P**1** and P**2** and to turn off the NMOS transistor N**3**. When the ESD event occurs at the I/O pad **60**, a portion of ESD energy from the I/O pad **60** sequentially passes through the diode D**3**, the power line VDD, the diode chain **50** and the PMOS transistor P**1**, to turn on the NMOS transistors N**2** and N**5**, and then passes through the PMOS transistor P**2** to turn on the NMOS transistors N**1** and N**4**, as shown in label S**6**. In ESD mode, a first discharge path is formed from the I/O pad **60** to the ground GND via the NMOS transistors N**4** and N**5**, and a second discharge path is formed from the I/O pad **60** to the ground GND via the diode D**3** and the NMOS transistors N**4** and N**5**. Thus, the electrical devices of the IC coupled to the power line VDD will be prevented from ESD damage. Similarly, the parasitic bipolar transistors and the parasitic resistors may provide additional discharge paths for the ESD protection circuit **600**.

FIG. **7** shows an ESD protection circuit **700** according to another embodiment of the invention, wherein the ESD protection circuit **700** is implemented in an IC. The ESD protection circuit **700** comprises the NMOS transistors N**1** and N**2**, a detection unit **30** and a trigger unit **70**. The detection unit **30** comprises the resistors R**1**, R**2**, R**3** and R**5** and a capacitor C, wherein the capacitor C is formed by an NMOS transistor. The resistor R**1** is coupled between the power line VDD and a gate of the NMOS transistor N**1**. The resistor R**2** is coupled between the ground GND and the gate of the NMOS transistor N**1**. The resistor R**3** is coupled between the power line VDD and the resistor R**5**. The resistor R**5** is coupled between the resistor R**3** and the ground GND. The capacitor C is coupled to the resistor R**5** in parallel. The trigger unit **70** comprises the PMOS transistors P**1** and P**2**, an NMOS transistor N**3** and a cascade unit **80**. The cascade unit **80** is coupled between the power line VDD and the PMOS transistor P**1**, which comprises a plurality of PMOS transistors P**3**. The PMOS transistors P**3** are cascaded between the power line VDD and the PMOS transistor P**1**. For each PMOS transistor P**3**, its bulk is coupled to its source, and its gate is coupled to its drain, thus the PMOS transistor P**3** functions as a diode. The amount of the PMOS transistors P**3** is determined according to actual applications. For example, the sum of the drain-to-source voltages of the PMOS transistors P**3** plus a threshold voltage of the PMOS transistor P**1** equals a voltage of the detection signal DET. In one embodiment, the cascade unit **80** may only comprise a single PMOS transistor P**3**. The PMOS transistor P**1** is coupled between the cascade unit **80** and a gate of the NMOS transistor N**2**. The PMOS transistor P**2** is coupled between the gates of the NMOS transistors N**1** and N**2**. The gates of the PMOS transistor P**1** and P**2** are coupled to the capacitor C for receiving a detection signal DET, and the bulks of the PMOS transistors P**1** and P**2** are coupled to the cascade unit **80** and the power line VDD, respectively. The NMOS transistor N**3** is coupled between the PMOS transistor P**1** and the ground GND, wherein a gate of the NMOS transistor N**3** is coupled to the capacitor C for receiving the detection signal DET. Similarly, the NMOS transistors **N1** and **N2** are stacked NMOS transistors for reliability, wherein the NMOS transistor **N1** is coupled between the power line VDD and the NMOS transistor **N2** and the NMOS transistor **N2** is coupled between the NMOS transistor **N1** and the ground GND. The gate of the NMOS transistor **N1** is controlled by a control signal CTRL**1**, and the gate of the NMOS transistor **N2** is controlled by a control signal CTRL**2**, wherein the bulks of the NMOS transistors **N1** and **N2** are coupled to the ground GND.

In FIG. **7**, the NMOS transistor **N1**, **N2** and **N3** and the PMOS transistors **P1**, **P2** and **P3** are low-voltage devices (e.g. 1.8V), and a higher fixed voltage (e.g. 3.3V) is applied to the power line VDD via a power pad of the IC. In normal mode, the control signal CTRL**1** is determined according to a voltage division between the resistors R**1** and R**2**, e.g. if R**1**=R**2**, CTRL**1**=VDD/2. Thus, the NMOS transistor **N1** is turned on. Furthermore, the detection signal DET is determined according to a voltage division between the resistors R**3** and R**5**, e.g. if R**3**=R**5**, DET=VDD/2. Therefore, the PMOS transistors **P1** and **P2** are turned off and the NMOS transistor **N3** is turned on, and then the control signal CTRL**2** is pulled down to the ground GND via the NMOS transistor **N3**. Thus, the NMOS transistor **N2** is turned off. When an ESD event occurs at the power line VDD, the detection unit **30** provides the detection signal DET in response to the ESD event, to turn on the PMOS transistors **P1** and **P2** and to turn off the NMOS transistor **N3**. Next, a portion of ESD energy from the power line VDD passes through the cascade unit **80** and the PMOS transistor **P1**, to turn on the NMOS transistor **N2**, and then passes through the PMOS transistor **P2** to turn on the NMOS transistor **N1**, as shown in label S**7**. Therefore, a discharge path is formed from the power line VDD to the ground GND via the NMOS transistors **N1** and **N2** in ESD mode, such that the electrical devices of the IC coupled to the power line VDD will be prevented from ESD damage. Furthermore, a parasitic bipolar transistor BJT and a parasitic resistor RP may provide an additional discharge path for the ESD protection circuit **700**.

FIG. **8** shows an ESD protection circuit **800** according to another embodiment of the invention, wherein the ESD protection circuit **800** is implemented in an IC. Compared to the ESD protection circuit **700** of FIG. **7**, the ESD protection circuit **800** is used to provide ESD protection for an I/O pad **60** of the IC. The ESD protection circuit **800** comprises a diode D**3**, the NMOS transistors **N4** and **N5**, a detection unit **30** and a trigger unit **70**, wherein details of the detection unit **30** and the trigger unit **70** are described above. An anode of the diode D**3** is coupled to the I/O pad **60** and a cathode of the diode D**3** is coupled to the power line VDD. The NMOS transistor **N4** is coupled between the anode of the diode D**3** and the NMOS transistor **N5**, which has a gate coupled to the resistors R**1** and R**2** and the PMOS transistor **P2** for receiving the control signal CTRL**1**. The NMOS transistor **N5** is coupled between the NMOS transistor **N4** and the ground GND, which has a gate coupled to the NMOS transistor **N3** and the PMOS transistors **P1** and **P2** for receiving the control signal CTRL**2**.

In FIG. **8**, the NMOS transistors **N4** and **N5** and the PMOS transistors **P1**, **P2** and **P3** are low-voltage devices (e.g. 1.8V), and a higher fixed voltage (e.g. 3.3V) is applied to the power line VDD via a power pad of the IC. In normal mode, the control signal CTRL**1** is determined according to a voltage division between the resistors R**1** and R**2**, e.g. if R**1**=R**2**, CTRL**1**=VDD/2. Thus, the NMOS transistor **N4** is turned on. Furthermore, the detection signal DET is determined according to a voltage division between the resistors R**3** and R**5**, e.g. if R**3**=R**5**, DET=VDD/2. Therefore, the PMOS transistors **P1** and **P2** are turned off and the NMOS transistor **N3** is turned on, and then the control signal CTRL**2** is pulled down to the ground GND via the NMOS transistor **N3**. Thus, the NMOS transistor **N5** is turned off. When an ESD event occurs at the I/O pad **60**, a portion of ESD energy from the I/O pad **60** passes through the diode D**3** to the power line VDD. Therefore, the detection unit **30** provides the detection signal DET in response to the ESD event, to turn on the PMOS transistors **P1** and **P2** and to turn off the NMOS transistor **N3**. When the ESD event occurs at the I/O pad **60**, a portion of ESD energy the I/O pad **60** sequentially passes through the diode D**3**, the power line VDD, the cascade unit **80** and the PMOS transistor **P1**, to turn on the NMOS transistor **N5**, and then passes through the PMOS transistor **P2** to turn on the NMOS transistor **N4**, as shown in label S**8**. Therefore, a discharge path is formed from the I/O pad **60** to the ground GND via the NMOS transistors **N4** and **N5** in an ESD mode, such that the electrical devices of the IC coupled to the power line VDD will be prevented from ESD damage. Similarly, a parasitic bipolar transistor and a parasitic resistor may further provide an additional discharge path for the ESD protection circuit **800**.

FIG. **9** shows an ESD protection circuit **900** according to another embodiment of the invention, wherein the ESD protection circuit **900** is implemented in an IC. Compared to the ESD protection circuit **800** of FIG. **8**, the ESD protection circuit **900** further comprises the NMOS transistors **N1** and **N2**. The NMOS transistor **N1** is coupled between the power line VDD and the NMOS transistor **N2**, which has a gate coupled to the gate of the NMOS transistor **N4**. The NMOS transistor **N2** is coupled between the NMOS transistor **N1** and the ground GND, which has a gate coupled to the gate of the NMOS transistor **N5**. In FIG. **9**, the NMOS transistors **N1**, **N2**, **N4** and **N5** and the PMOS transistors **P1**, **P2** and **P3** are low-voltage devices (e.g. 1.8V), and a higher fixed voltage (e.g. 3.3V) is applied to the power line VDD via a power pad of the IC. In normal mode, the control signal CTRL**1** is determined according to a voltage division between the resistors R**1** and R**2**, e.g. if R**1**=R**2**, CTRL**1**=VDD/2. Thus, the NMOS transistors **N1** and **N4** are turned on. Furthermore, the detection signal DET is determined according to a voltage division between the resistors R**3** and R**5**, e.g. if R**3**=R**5**, DET=VDD/2. Therefore, the PMOS transistors **P1** and **P2** are turned off and the NMOS transistor **N3** is turned on, and then the control signal CTRL**2** is pulled down to the ground GND via the NMOS transistor **N3**. Thus, the NMOS transistors **N2** and **N5** are turned off. When an ESD event occurs at the I/O pad **60**, a portion of ESD energy from the I/O pad **60** passes through the diode D**3** to the power line VDD. Therefore, the detection unit **30** provides the detection signal DET in response to the ESD event, to turn on the PMOS transistors **P1** and **P2** and to turn off the NMOS transistor **N3**. When the ESD event occurs at the I/O pad **60**, a portion of ESD energy from the I/O pad **60** sequentially passes through the diode D**3**, the power line VDD, the cascade unit **80** and the PMOS transistor **P1**, to turn on the NMOS transistors **N2** and **N5**, and then passes through the PMOS transistor **P2** to turn on the NMOS transistors **N1** and **N4**, as shown in label S**9**. In ESD mode, a first discharge path is formed from the I/O pad **60** to the ground GND via the NMOS transistors **N4** and **N5**, and a second discharge path is formed from the I/O pad **60** to the ground GND via the diode D**3** and the NMOS transistors **N4** and **N5**. Thus, the electrical devices of the IC coupled to the power line VDD will be prevented from ESD damage. Similarly, the parasitic bipolar transistors and the parasitic resistors may provide additional discharge paths for the ESD protection circuit **900**.

While the invention has been described by way of example and in terms of the preferred embodiments, it is to be understood that the invention is not limited to the disclosed embodiments. On the contrary, it is intended to cover various modifications and similar arrangements (as would be apparent to those skilled in the art). Therefore, the scope of the appended claims should be accorded the broadest interpretation so as to encompass all such modifications and similar arrangements.

What is claimed is:

1. An electrostatic discharge (ESD) protection circuit, comprising:

a first NMOS transistor coupled to a power line;

a second NMOS transistor coupled between the first NMOS transistor and a ground;

a detection unit, providing a detection signal when an ESD event occurs at the power line; and

a trigger unit, turning on the second NMOS transistor and the first NMOS transistor in sequence in response to the detection signal, such that a discharge path is formed from the power line to the ground via the first and second NMOS transistors, wherein the trigger unit comprises:

a first PMOS transistor coupled between the power line and a gate of the second NMOS transistor, having a gate coupled to the detection unit for receiving the detection signal;

a third NMOS transistor coupled between the ground and the gate of the second NMOS transistor, having a gate coupled to the gate of the first PMOS transistor;

a second PMOS transistor coupled between a gate of the first NMOS transistor and the gate of the second NMOS transistor, having a gate coupled to the gate of the first PMOS transistor; and

a third PMOS transistor coupled between the power line and the first PMOS transistor, having a drain, a gate, and a source, wherein the drain is coupled to the gate and the first PMOS transistor, and the source is coupled to the power line.

2. The ESD protection circuit as claimed in claim **1**, wherein the first and second PMOS transistors are turned off by the detection signal when the ESD event is absent, wherein the first NMOS transistor is turned on by the detection unit and the second NMOS transistor is turned off by the third NMOS transistor when the ESD event is absent.

3. The ESD protection circuit as claimed in claim **1**, wherein the detection unit comprises:

a first resistor coupled between the power line and the gate of the first NMOS transistor;

a second resistor coupled between the gate of the first NMOS transistor and the ground;

a third resistor coupled between the power line and the gate of the first PMOS transistor;

a fourth resistor coupled between the third resistor and the ground; and

a capacitor coupled to the fourth resistor in parallel.

4. The ESD protection circuit as claimed in claim **1**, wherein when the ESD event occurs, the first and second PMOS transistors are turned on by the detection signal, wherein the second NMOS transistor is turned on by ESD energy from the power line through the first PMOS transistor, and the second NMOS transistor is turned on by ESD energy from the power line through the first PMOS transistor and the second PMOS transistor.

5. The ESD protection circuit as claimed in claim **1**, further comprising:

a parasitic bipolar transistor and a parasitic resistor, coupled between the power line and the ground,

wherein another discharge path is formed from the power line to the ground via the parasitic bipolar transistor and the parasitic resistor.

6. An electrostatic discharge (ESD) protection circuit, comprising:

a diode, having an anode coupled to a pad and a cathode coupled to a power line;

a first NMOS transistor coupled to the pad;

a second NMOS transistor coupled between the first NMOS transistor and a ground;

a detection unit coupled between the power line and the ground, providing a detection signal when an ESD event occurs at the pad; and

a trigger unit coupled between the power line and the ground, turning on the second NMOS transistor and the first NMOS transistor in sequence in response to the detection signal, such that a first discharge path is formed from the pad to the ground through the first and second NMOS transistors, wherein the trigger unit comprises:

a first PMOS transistor coupled between the power line and a gate of the second NMOS transistor, having a gate coupled to the detection unit for receiving the detection signal;

a third NMOS transistor coupled between the ground and the gate of the second NMOS transistor, having a gate coupled to the gate of the first PMOS transistor;

a second PMOS transistor coupled between a gate of the first NMOS transistor and the gate of the second NMOS transistor, having a gate coupled to the gate of the first PMOS transistor; and

a third PMOS transistor coupled between the power line and the first PMOS transistor, having a drain, a gate, and a source, wherein the drain is coupled to the gate and the first PMOS transistor, and the source is coupled to the power line.

7. The ESD protection circuit as claimed in claim **6**, wherein the first and second PMOS transistors are turned off by the detection signal when the ESD event is absent, wherein the first NMOS transistor is turned on by the detection unit and the second NMOS transistor is turned off by the third NMOS transistor when the ESD event is absent.

8. The ESD protection circuit as claimed in claim **6**, wherein the detection unit comprises:

a first resistor coupled between the power line and the gate of the first NMOS transistor;

a second resistor coupled between the gate of the first NMOS transistor and the ground;

a third resistor coupled between the power line and the gate of the first PMOS transistor;

a fourth resistor coupled between the third resistor and the ground; and

a capacitor coupled to the fourth resistor in parallel.

9. The ESD protection circuit as claimed in claim **6**, wherein when the ESD event occurs, the first and second PMOS transistors are turned on by the detection signal, wherein the second NMOS transistor is turned on by ESD energy from the pad sequentially through the first diode, the power line and the first PMOS transistor, and the second NMOS transistor is turned on by ESD energy from the pad sequentially through the first diode, the power line, the first PMOS transistor and the second PMOS transistor.

10. The ESD protection circuit as claimed in claim **6**, further comprising:

a fourth NMOS transistor coupled to the power line, having a gate coupled to the gate of the first NMOS transistor; and a fifth NMOS transistor coupled between the fourth NMOS transistor and the ground, having a gate coupled to the gate of the second NMOS transistor,

wherein the fifth NMOS transistor and the fourth NMOS transistor are turned on in sequence in response to the detection signal, such that a second discharge path is formed from the pad to the ground through the first diode and the third and fourth NMOS transistors.

11. An electrostatic discharge (ESD) protection circuit, comprising:

a first NMOS transistor coupled to a power line;

a second NMOS transistor coupled between the first NMOS transistor and a ground;

a detection unit, providing a detection signal when an ESD event occurs at the power line; and

a trigger unit, turning on the second NMOS transistor and the first NMOS transistor in sequence in response to the detection signal, such that a discharge path is formed from the power line to the ground via the first and second NMOS transistors, wherein the trigger unit comprises:

a first PMOS transistor coupled between the power line and a gate of the second NMOS transistor, having a gate coupled to the detection unit for receiving the detection signal;

a third NMOS transistor coupled between the ground and the gate of the second NMOS transistor, having a gate coupled to the gate of the first PMOS transistor;

a second PMOS transistor coupled between a gate of the first NMOS transistor and the gate of the second NMOS transistor, having a gate coupled to the gate of the first PMOS transistor; and

a plurality of third PMOS transistors coupled between the power line and the first PMOS transistor in serial, each having a drain, a gate, a source and a bulk, wherein the drain of the third PMOS transistor is coupled to the gate thereof, and the source of the third PMOS transistor is coupled to the bulk thereof.

12. The ESD protection circuit as claimed in claim **11**, wherein the first and second PMOS transistors are turned off by the detection signal when the ESD event is absent, wherein the first NMOS transistor is turned on by the detection unit and the second NMOS transistor is turned off by the third NMOS transistor when the ESD event is absent.

13. The ESD protection circuit as claimed in claim **11**, wherein the detection unit comprises:

a first resistor coupled between the power line and the gate of the first NMOS transistor;

a second resistor coupled between the gate of the first NMOS transistor and the ground;

a third resistor coupled between the power line and the gate of the first PMOS transistor;

a fourth resistor coupled between the third resistor and the ground; and

a capacitor coupled to the fourth resistor in parallel.

14. The ESD protection circuit as claimed in claim **11**, wherein when the ESD event occurs, the first and second PMOS transistors are turned on by the detection signal, wherein the second NMOS transistor is turned on by ESD energy from the power line through the first PMOS transistor, and the second NMOS transistor is turned on by ESD energy from the power line through the first PMOS transistor and the second PMOS transistor.

15. The ESD protection circuit as claimed in claim **11**, further comprising:

a parasitic bipolar transistor and a parasitic resistor, coupled between the power line and the ground,

wherein another discharge path is formed from the power line to the ground via the parasitic bipolar transistor and the parasitic resistor.

16. An electrostatic discharge (ESD) protection circuit, comprising:

a diode, having an anode coupled to a pad and a cathode coupled to a power line;

a first NMOS transistor coupled to the pad;

a second NMOS transistor coupled between the first NMOS transistor and a ground;

a detection unit coupled between the power line and the ground, providing a detection signal when an ESD event occurs at the pad; and

a trigger unit coupled between the power line and the ground, turning on the second NMOS transistor and the first NMOS transistor in sequence in response to the detection signal, such that a first discharge path is formed from the pad to the ground through the first and second NMOS transistors, wherein the trigger unit comprises:

a first PMOS transistor coupled between the power line and a gate of the second NMOS transistor, having a gate coupled to the detection unit for receiving the detection signal;

a third NMOS transistor coupled between the ground and the gate of the second NMOS transistor, having a gate coupled to the gate of the first PMOS transistor;

a second PMOS transistor coupled between a gate of the first NMOS transistor and the gate of the second NMOS transistor, having a gate coupled to the gate of the first PMOS transistor; and

a plurality of third PMOS transistors coupled between the power line and the first PMOS transistor, each having a drain, a gate, a source and a bulk, wherein the drain of the third PMOS transistor is coupled to the gate thereof, and the source of the third PMOS transistor is coupled to the bulk thereof.

17. The ESD protection circuit as claimed in claim **16**, wherein the first and second PMOS transistors are turned off by the detection signal when the ESD event is absent, wherein the first NMOS transistor is turned on by the detection unit and the second NMOS transistor is turned off by the third NMOS transistor when the ESD event is absent.

18. The ESD protection circuit as claimed in claim **16**, wherein the detection unit comprises:

a first resistor coupled between the power line and the gate of the first NMOS transistor;

a second resistor coupled between the gate of the first NMOS transistor and the ground;

a third resistor coupled between the power line and the gate of the first PMOS transistor;

a fourth resistor coupled between the third resistor and the ground; and

a capacitor coupled to the fourth resistor in parallel.

19. The ESD protection circuit as claimed in claim **16**, wherein when the ESD event occurs, the first and second PMOS transistors are turned on by the detection signal, wherein the second NMOS transistor is turned on by ESD energy from the pad sequentially through the first diode, the power line and the first PMOS transistor, and the second NMOS transistor is turned on by ESD energy from the pad sequentially through the first diode, the power line, the first PMOS transistor and the second PMOS transistor.

20. The ESD protection circuit as claimed in claim **16**, further comprising:

a fourth NMOS transistor coupled to the power line, having a gate coupled to the gate of the first NMOS transistor; and

a fifth NMOS transistor coupled between the fourth NMOS transistor and the ground, having a gate coupled to the gate of the second NMOS transistor,

wherein the fifth NMOS transistor and the fourth NMOS transistor are turned on in sequence in response to the detection signal, such that a second discharge path is formed from the pad to the ground through the first diode and the third and fourth NMOS transistors.

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